SiFive-ARTY Adapter

Timeline

Overview

The SiFive-ARTY Adapter allows debug connections between J-Link and the ARTY board running SiFive RISC-V core bitstreams. The ARTY board provides several identical headers where the JD header is used as the debug connector, when running SiFive RISC-V bitstreams on the ARTY board.

Pin out

Pin	Signal
1	NC
2	VTref / VDD
3	NC
4	GND
5	NC
6	NC
7	тск
8	RESET
9	TRST
10	TMS
11	TDO
12	TDI

Key features

 Allows debug connections between J-Link and ARTY board

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USR

LAW

link

Order number

8.06.24



